HW 7: Band Energy using FFT
CMPE 415 UMBC

April 29, 2016

For this lab, your goal is to implement a calculation of signal band energy. Six bands are to be defined by ranges of FFT indexes, [Lower Index, Upper Index], based on a 1024-point transform.

The computer will first send band specifications in this format:

Table 1: Band Definition Format (Sent from Computer to FPGA)

Byte 0	ASCII 'B'
Byte 1	Bin Number 0-5
Byte 2	Lower Index High Byte
Byte 3	Lower Index Low Byte
Byte 4	Upper Index High Byte
Byte 5	Upper Index Low Byte

Note, the bounds of the bands are inclusive and may be overlapping. (Some of you may know that the second half of the coefficients are redundant, but assume ignorance for this exercise)

The reported value for each band should be the sum of the squares of both the real and imaginary results for all index corresponding to values in the bins.

$$\text{Band Energy } = \sum_{\text{index=Lower Index}}^{\text{index=Upper Index}} \left((xk\_re[index])^2 + (xk\_im[index])^2 \right)$$

The result should be computed using 32 bit results for additions and multiplications, however there is an extra stipulation for this exercise: **Your code should implement this calculation, including intermediate results and final result storage, entirely inside a single case-state based state machine description, using no more than more than a single 16-bit-input hardware multiplication being performed in a given clock cycle.**

The final results (6 energy values) shall be reported through the serial port using the following format:

Table 2: Band Energy Format (Sent from FPGA to Computer)

Byte 0	ASCII 'E'
Byte 1	Bin Number 0-5
Byte 2	Result Byte 3 (MSB)
Byte 3	Result Byte 2
Byte 4	Result Byte 1
Byte 5	Result Byte 0 (LSB)

Based on this specification, for each transform operation you will report a total of 6 bins using 6 bytes each, for a total of 32 bytes.

You may test your design using the serial port to send 1024 values of two byes each to the FFT transform. You will submit the usual report with discussions on testbenches, hardware evaluations, design choices, and code implementation.

Extra Credit 10 Points:

Collect input samples from the onboard ADC instead of the serial port at 40 kHz.

The incoming signal from the ADC is documented in the user guide.

https://reference.digilentinc.com/_media/s3e:s3estarter_ug.pdf#page=78

The ADC first waits on a small pulse to start a conversion. It then shifts data out 1-bit at a time based on a clock signal provided to it.

Your goal is to trigger the conversions at a rate near 40 kHz and capture the data. A continuous stream of data can be support, but if you cannot manage it then it is better to implement burst captures at 40 kHz with breaks between then implement other irregular sampling intervals.

The data should then be provided to the FFT transform and the results report per the specification provided already in the assignment.