Placing a FET in series such that we are examining the resistance looking into the source tends to lower the effective resistance.

\[ R_{\text{eff}} = \frac{R_D + r_{ds}}{1 + g_s r_{ds}} \]
Looking into source, FET behaves as a current buffer:

- reducing input voltage variation w/current (low input resistance)
- shielding input from variations of voltage on output
- providing high output resistance on the output drain side
Placing a FET in series such that we are looking into the drain tends to have a higher resistance. The current changes less when the voltage changes.

\[ R_{eff} = g_s r_{ds} R_S + r_{ds} + R_S \]

henceforth to be known as the cascode equation.
Common Source Amplifier:
\[ G_m = -g_m \]
\[ R_{out} = R_D \parallel r_{ds} \]
Increasing \( R_D \) increases \( A_v \), \( R_{out} < r_{ds} \)

Casced C.S. Amplifier:
Assume sat. for both FETs
Use Cascode Equation
\[ R_{out} = R_D \parallel g_{s2} r_{ds2} r_{ds1} + r_{o2} + r_{o1} \]
Under common assumptions (be able to state them)
\[ R_{out} \approx R_D \parallel g_{s2} r_{ds2} r_{ds1} \]
Now \( R_{out} \) can be much larger as \( R_D \) is increased (But remember \( R_{out} C_{out} \) increases, possibly reducing BW)
Use current division equation:
\[ i_y = -v_i g_m \cdot \left( \frac{r_{ds1}}{r_{ds1} + \frac{1}{g_{s2}}} \right) \]
\[ G_m = \frac{i_y}{v_i} = -g_{m1} \cdot \left( \frac{r_{ds1}}{r_{ds1} + \frac{1}{g_{s2}}} \right) \]
if \( \frac{1}{g_{s2}} \ll r_{ds1} \),
\[ G_m \approx -g_{m1} \]
High-$r_{ds}$

Large $V_{DS,SAT}$

Approximately same $g_m$

May allow higher DC gain due to larger output resistance, perhaps with associated cost of BW
Effect on output range and how to set $V_{\text{cas}}$

- **M2 sat condition**: $V_{\text{out}} \geq V_{\text{cas}} - V_{TH2} = V_{out,min}$
  - When $V_{\text{out}} < V_{\text{cas}} - V_{TH2}$, $r_{ds2}$ and $g_{s2}$ reduce, causing the gain to reduce. This causes a distortion.

- **M1 sat condition**: $V_x > V_{\text{in,bias}} - V_{TH1}, V_x > V_{ov1}$
  - $(V_{\text{in,bias}}$ is designed though $I_{bias}, \left(\frac{W}{L}\right)_1)$
Effect on output range and how to set $V_{cas}$

- $V_{cas}$ is a design variable. To design we must examine $V_x$:
  - node $V_x$ is typically a low resistance node and does not change in voltage much as the current of $M1$ is changed

- $V_{cas}$ must support the bias current through $M2$ requiring some potential above the source:
  - $V_{cas} - V_x - V_{TH2} = V_{OV2}$
  - $V_{cas} = V_{ov2} + V_{TH2}$ (threshold plus overdrive)
  - Thus $V_{cas} - V_x > V_{ov1} + V_{ov2} + V_{TH2}$

- As $V_{cas}$ is set, $V_x$ tends to follow it according to the source follower behavior:
Effect on output range and how to set $V_{cas}$

- If $V_{cas}$ is set too low, $V_x$ is pushed below $V_{ov1}$ and M1 leaves sat
  - (Design tip: if you run DC sim and find that M1 is not sat, increase $V_{cas}$)
- If $V_{cas}$ is set too high, it needlessly limit $V_{out}$ (sets $V_{out,min}$) and jeopardizes M2 sat
- Output Limitation:
  - $V_{out} > V_{out,min} = V_{cas} - V_{TH2}$
  - BEST CASE:
    - $V_{cas} = V_{ov1} + V_{ov2} + V_{TH2}$
    - $V_{out,min} = V_{ov1} + V_{ov2}$
- Common mistake: assume $V_{out,min} = V_{ov1} + V_{ov2}$ without considering actual value of $V_{cas}$
  - (I tend to ask a related question on exams)
Study effect of M2 on $A_v$ in two parts:

- M2 effect on $R_{OUT}$?
  - Non-cascoded: $R_{out} = r_{ds3} || r_{ds1}$ maybe $\frac{r_{ds}}{2}$
  - Cascoded: $R_{out} = r_{ds3} || r_{ds1}g_{s2} r_{ds2} + r_{ds1} + r_{ds2}$ maybe $r_{ds}$
  - So effect on $R_{OUT}$ is not large
Example Circuit:

- Effect on GM:
  - Non-cascoded: $G_m = g_m$
  - Cascoded: $G_m = -g_{m1} \frac{g_{s2} + \frac{1}{r_{ds2}}}{g_{s2} + \frac{1}{r_{ds2}} + \frac{1}{r_{ds1}}} \approx -g_{m1}$
  - So effect on is very small

So, “one-sided” cascode does not have a large effect overall
\[ R_{out} = (r_{ds3}g_{s3}r_{ds4} + r_{ds3} + r_{ds4}) || (r_{ds1}g_{s2}r_{ds2} + r_{ds1} + r_{ds2}) \]

\[ R_{out} \approx (r_{ds3}g_{s3}r_{ds4}) || (r_{ds1}g_{s2}r_{ds2}) \]

\[ R_{out} \approx \frac{1}{2} g_s r_{ds}^2 \]

\[ G_m = -g_{m1} \frac{g_{s2} + \frac{1}{r_{ds2}} + \frac{1}{r_{ds1}}}{g_{s2} + \frac{1}{r_{ds2}} + \frac{1}{r_{ds1}}} \approx -g_{m1} \]
Non-cascoded: \[ A_V = g_m \frac{1}{2} r_d \]

Casced: \[ A_{V,\text{cas}} = g_m \frac{1}{2} g_s r_{ds}^2 \]

\[ \frac{A_{V,\text{cas}}}{A_V} = g_s r_{ds} \]

- (gain multiplied by intrinsic gain)
- (sometimes thought of as two gain stages)
\[ V_{casn} - V_{TH2} = V_{out,\, min} < V_{out} < V_{out,\, max} = V_{casp} + |V_{TH3}| \]

- Best case allows output to reach within two overdrive voltages of supply rails:
  - If this condition on \( V_{casn} \) AND \( V_{casp} \) is TRUE:
    - \( V_{casn} = V_{TH1} + V_{ov1} + V_{TH2} + V_{ov2} \) and
      \( V_{casp} = V_{DD} - |V_{TH4}| - V_{ov4} - |V_{TH3}| - V_{ov3} \)
  - Then:
    - Best case is achieved:
      \( V_{ov1} + V_{ov2} < V_{out} < V_{dd} - V_{ov2} - V_{ov3} \)
- I define PFET overdrive voltages as \( V_s - V_g - |V_{THp}| \) to keep the values typically positive
DC Transfer Curve

Transfer Function

Temporal Sin. Response

- Linear model
- Actual

Voltage

- $V_{casp} - V_{TH1}$
- $V_{casp}$
- $V_{cass}$

$M3$ Leaks Saturation

$M3$ Leaves Saturation

Linear model prediction

DC op. point for linearization

$V_{out}$

$V_{in}$
Overall Points for Fully Cascoded Amplifier

- Output range:
  - about a loss of two overdrive voltages (one toward each supply rail) as compared to non-cascoded version
- Gain:
  - multiplied by intrinsic gain
- $R_{out}$:
  - multiplied by intrinsic gain
- BW:
  - due to increased $R_{out}$, possible loss of BW, divided by intrinsic gain
Circuit Debugging notes/tips:

- **M1 not sat:**
  - Try increase $V_{casn}$ to raise $VD1$ or
  - decreasing $V_{ov1}$ or $V_{ov2}$

- **M4 not sat:**
  - Try decrease $V_{casp}$ to lower $VD4$ or
  - decrease $V_{ov3}$ or $V_{ov4}$

- **M2 not sat:**
  - try decrease $V_{casn}$ or
  - decrease $V_{ov2}$ or
  - decrease $V_{casn}$ and $V_{ov1}$

- **M3 not sat:**
  - try decrease $V_{casp}$ or
  - decrease $V_{ov3}$ or
  - increase $V_{casp}$ and decrease $V_{ov4}$

How to affect a given $V_{OV}$? Consider $\frac{W}{L}$ and $I_{bias}$
Note decreasing $V_{ov1}$ means lower input voltage bias point