Lecture 05: Cascode Configuration

Analog IC Design

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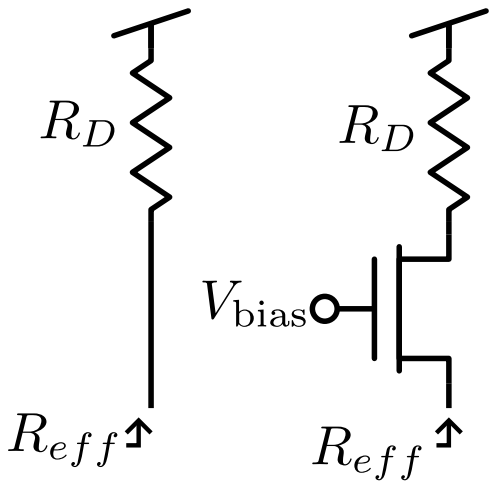
Lowered Resistance Looking into Source



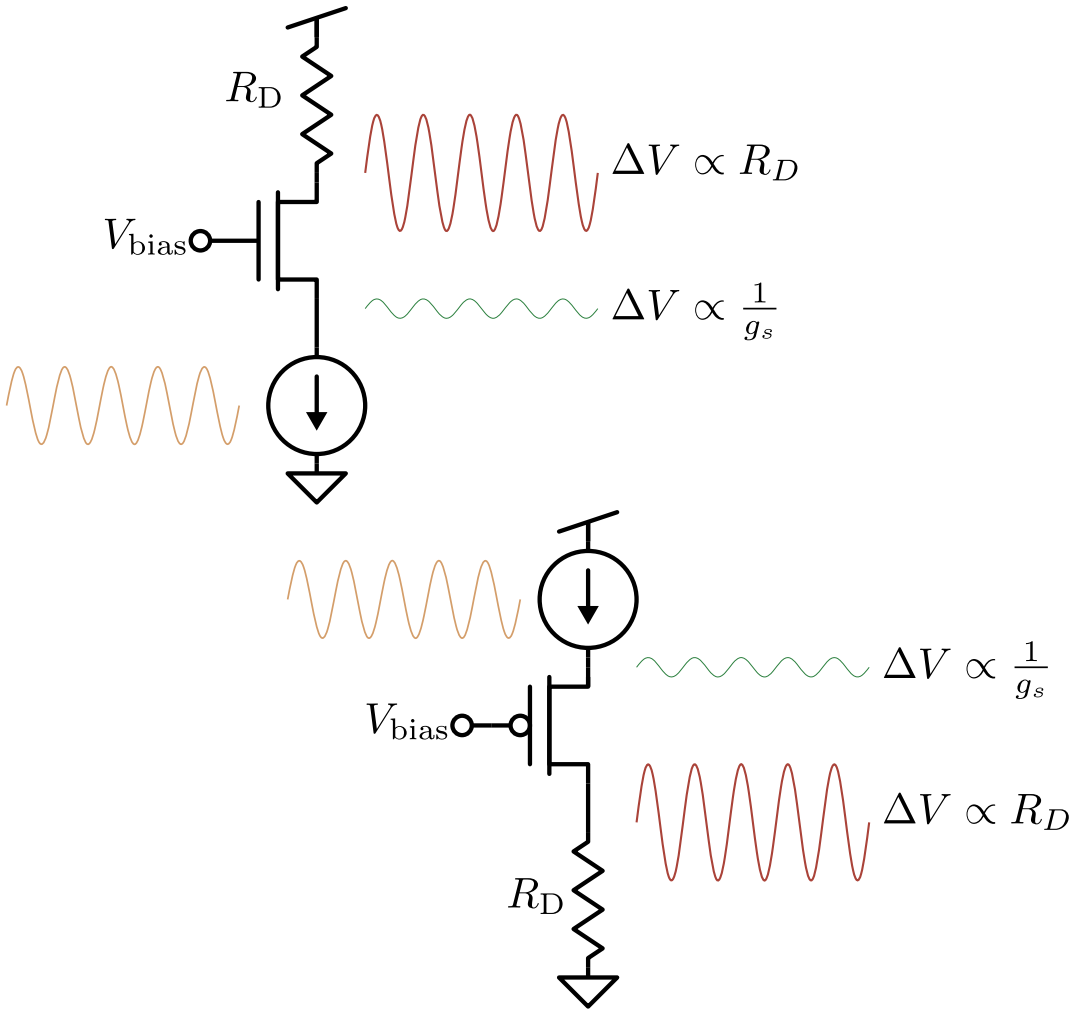
Placing a FET in series such that we are examining the resistance looking into the source tends to lower the effective resistance.

$$R_{eff} = \frac{R_D + r_{ds}}{1 + g_s r_{ds}}$$

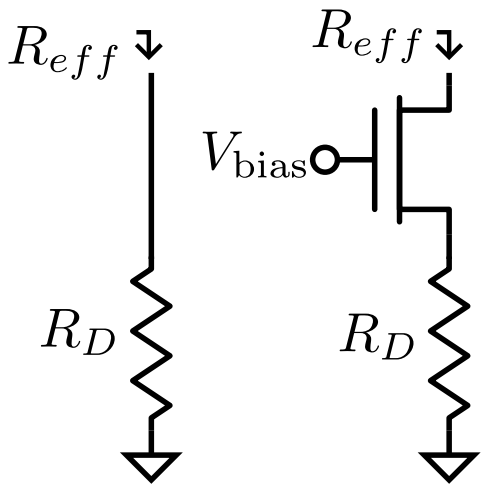
Current Buffer and Shielding

Looking into source, FET behaves as a current buffer

- reducing input voltage variation w/current (low input resistance)
- shielding input from variations of voltage on output
- providing high output resistance on the output drain side



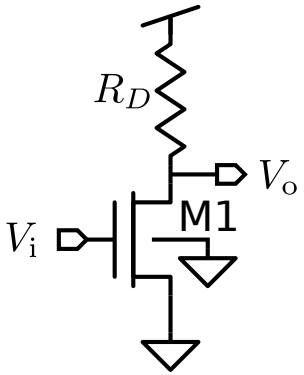
Cascode Configuration (looking into drain)

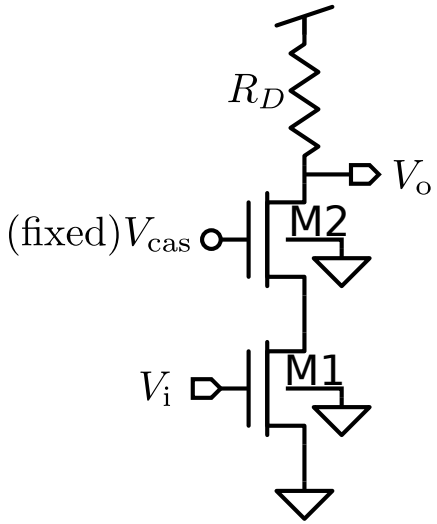


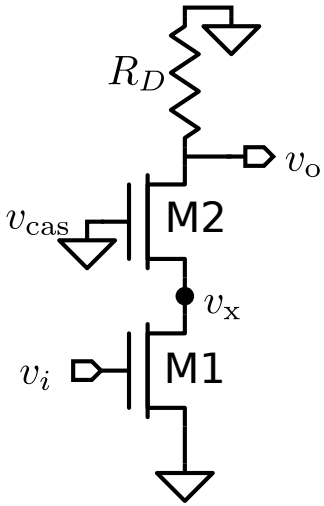
Placing a FET in series such that we are looking into the drain tends to have a higher resistance. The current changes less when the voltage changes.

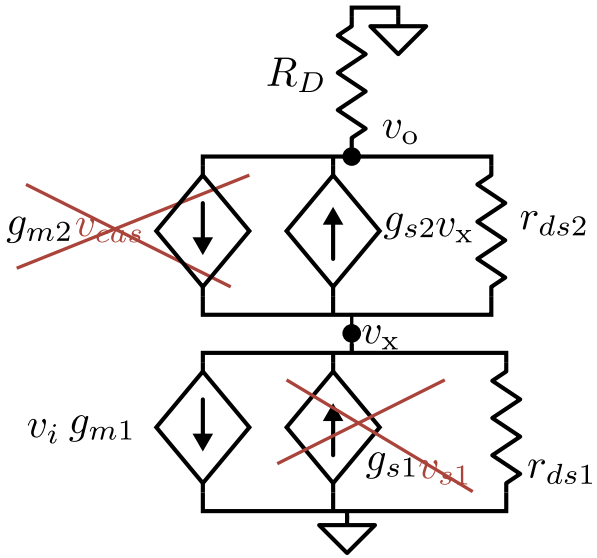
$R_{eff} = g_s r_{ds} R_S + r_{ds} + R_S$ henceforth to be known as the cascode equation

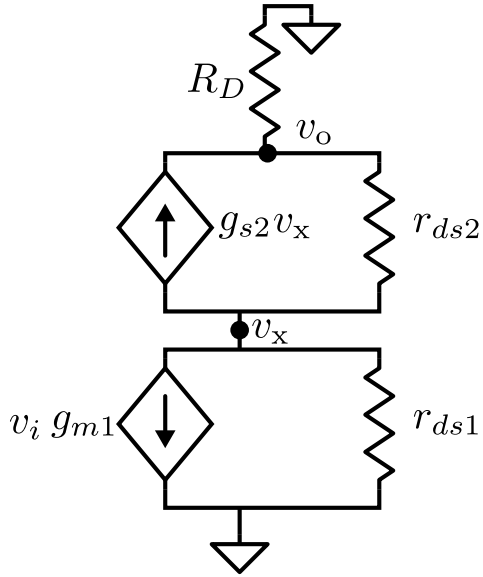
Cascoded C.S. Amplifier











Cascoded C.S. Amplifier

Common Source Amplifier:

$G_m = -g_m$

$R_{out} = R_D || r_{ds}$

Increasing R_D increases A_v,

$R_{out} < r_{ds}$

Cascoded C.S. Amplifier:

Assume sat. for both FETs

Use Cascode Equation

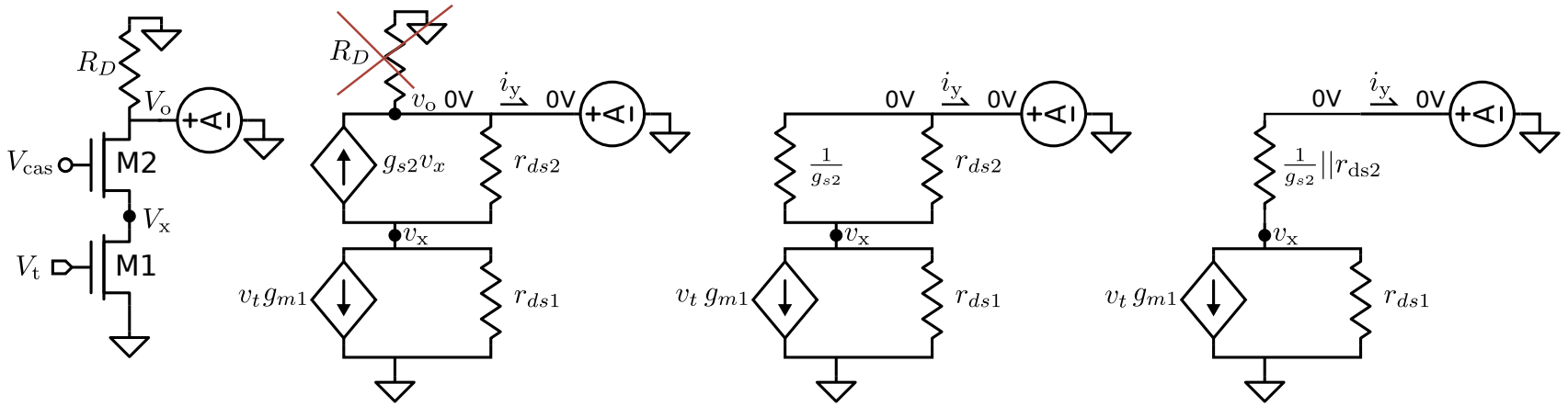
$R_{out} = R_D || g_{s2} r_{ds2} r_{ds1} + r_{o2} + r_{o1}$

Under common assumptions (be able to state them)

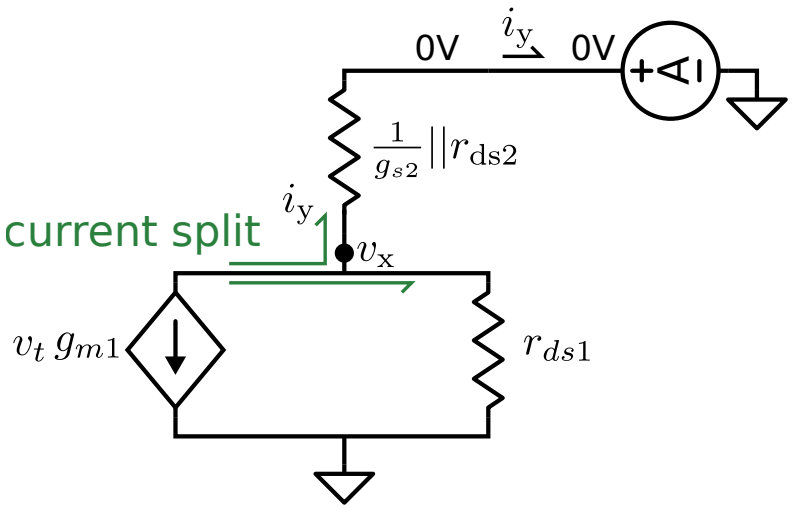
$R_{out} \approx R_D || g_{s2} r_{ds2} r_{ds1}$

Now R_{out} can be much larger as R_D is increased (But remember $R_{out} C_{out}$ increases, possibly reducing BW)

Cascode Effect on Gm



Use current division equation:



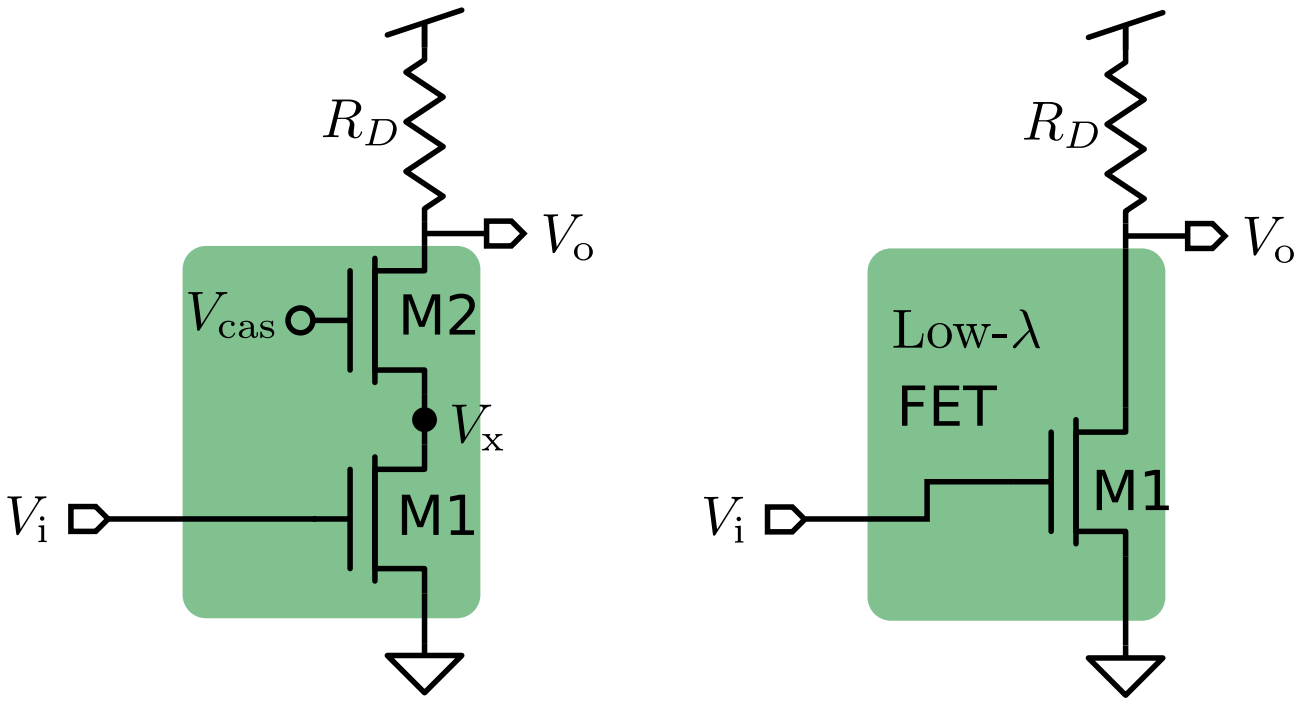
$$i_y = -v_i g_{m1} \cdot \left(\frac{r_{ds1}}{r_{ds1} + \frac{1}{g_{s2}} || r_{ds2}} \right)$$

$$G_m = \frac{i_y}{v_i} = -g_{m1} \cdot \left(\frac{r_{ds1}}{r_{ds1} + \frac{1}{g_{s2}} || r_{ds2}} \right)$$

if $\frac{1}{g_{s2}} \ll r_{ds1}$,

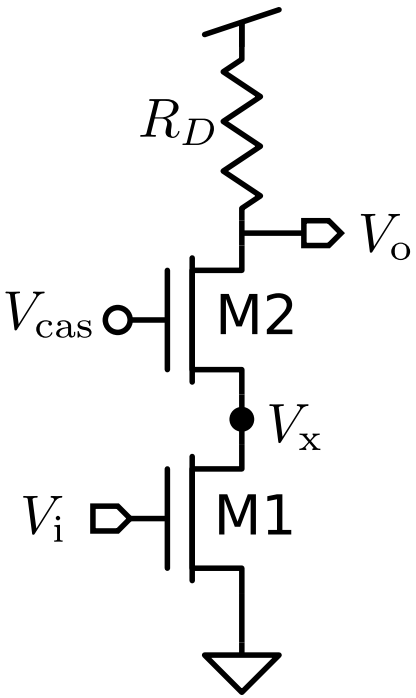
$G_m \approx -g_{m1}$

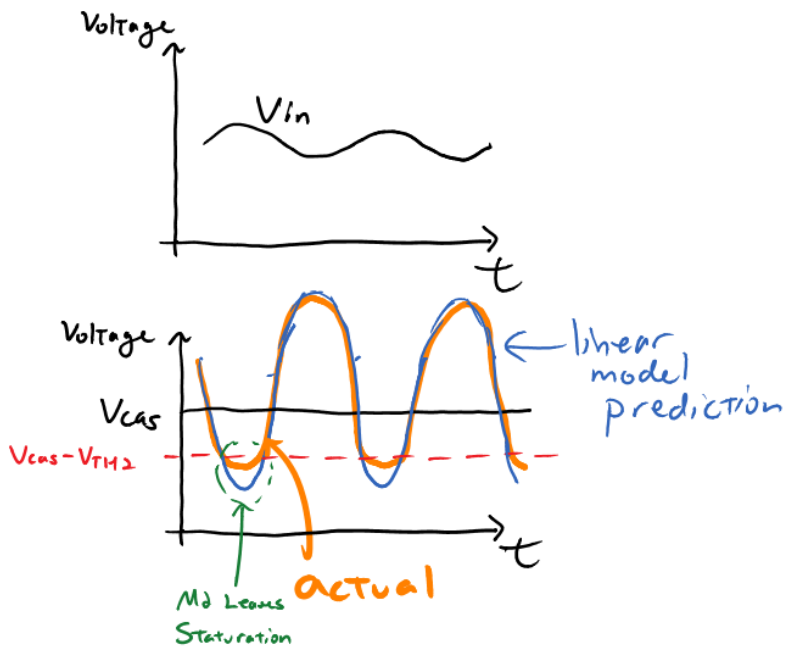
Cascode: Effective High-r_{ds} FET



- High-r_{ds}
- Large $V_{DS,SAT}$
- Approximately same g_m
- May allow higher DC gain due to larger output resistance, perhaps with associated cost of BW

Effect on output range and how to set Vcas

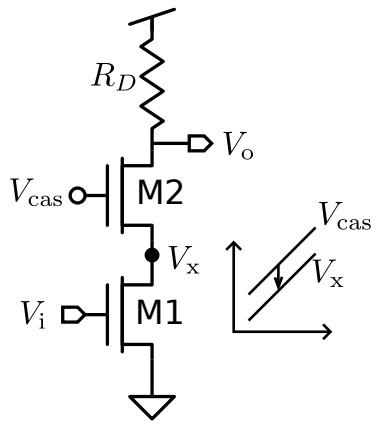




- M2 sat condition: $V_{out} >= V_{cas} - V_{TH2} = V_{out,min}$
  - When $V_{out} < V_{cas} - V_{TH2}$, $r_{ds2}$and g_{s2} reduce, causing the gain to reduce. This causes a distortion.
- M1 sat condition: $V_x > V_{in,bias} - V_{TH1}$, $V_x > V_{ov1}$
  - ($V_{in,bias}$ is designed though I_{bias}, $\left(\frac{W}{L}\right)_1$)

Effect on output range and how to set Vcas

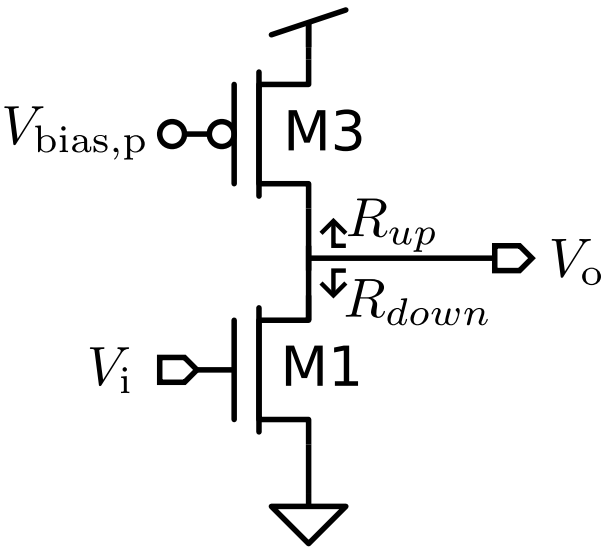
- V_{cas} is a design variable. To design we must examine V_x:
  - node V_x is typically a low resistance node and does not change in voltage much as the current of $M1$ is changed
- V_{cas} must support the bias current through M2 requiring some potential above the source:
  - $V_{cas} - V_x - V_{TH2} = V_{OV2}$
  - $V_{cas} = V_{ov2} + V_{TH2}$ (threshold plus overdrive)
    Thus $V_{cas} - V_x > V_{ov1} + V_{ov2} + V_{TH2}$
- As V_{cas} is set, V_x tends to follow it according to the source follower behavior:

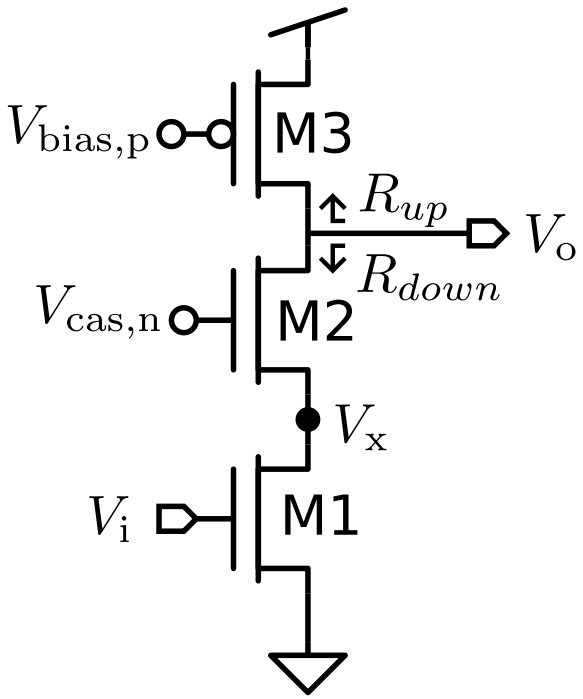


Effect on output range and how to set Vcas

- If V_{cas} is set too low, V_x is pushed below V_{ov1} and M1 leaves sat
  - (Design tip: if you run DC sim and find that M1 is not sat, increase V_{cas})
- If V_{cas} is set too high, it needlessly limit V_{out} (sets $V_{out,min}$) and jeopardizes M2 sat
- Output Limitation:
  - $V_{out} > V_{out,min} = V_{cas} - V_{TH2}$
  - BEST CASE:
    - $V_{cas} = V_{ov1} + V_{ov2} + V_{TH2}$
    - $V_{out,min} = V_{ov1} + V_{ov2}$
- Common mistake: assume $V_{out,min} = V_{ov1} + V_{ov2}$ without considering actual value of V_{cas}
  - (I tend to ask a related question on exams)

Example Circuit:





Study effect of M2 on A_v in two parts:

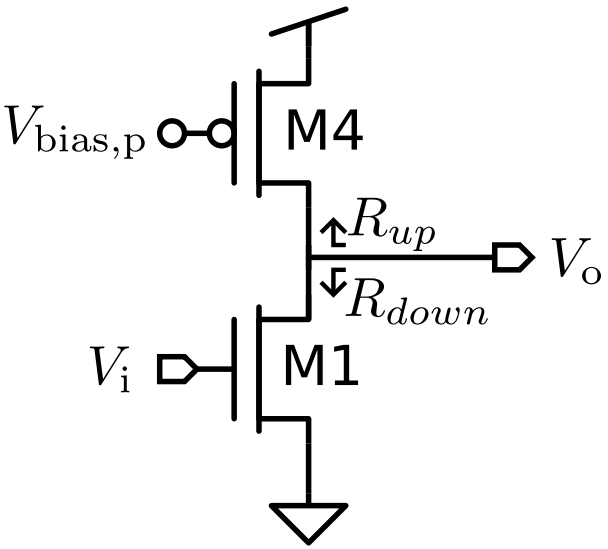
- M2 effect on R_{OUT}?
  - Non-cascoded: $R_{out} = r_{ds3}||r_{ds1}$ maybe $\frac{r_{ds}}{2}$
  - Cascoded: $R_{out} = r_{ds3}||r_{ds1}g_{s2}r_{ds2} + r_{ds1} + r_{ds2}$ maybe r_{ds}
  - So effect on R_{OUT} is not large

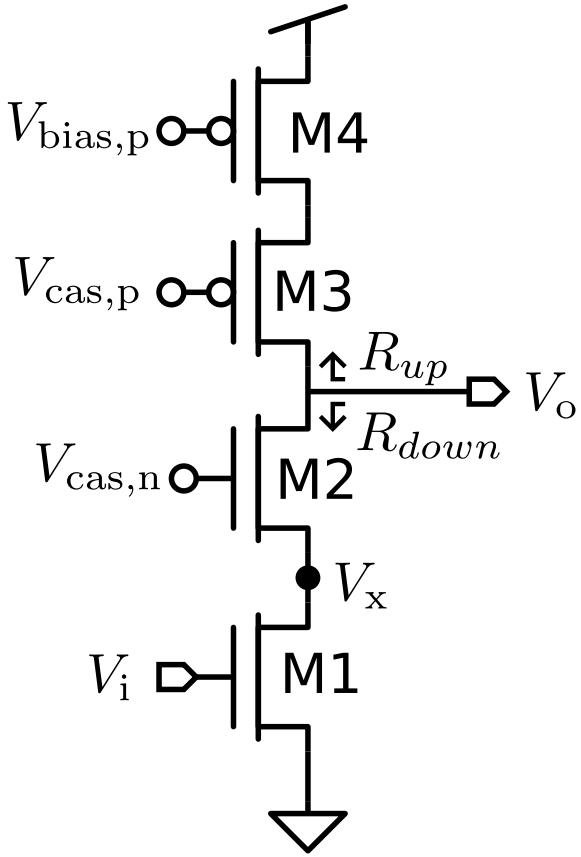
Example Circuit:

- Effect on GM:
  - Non-cascoded: $G_m = g_m$
  - Cascoded: $G_m = -g_{m1} \frac{g_{s2} + \frac{1}{r_{ds2}}}{g_{s2} + \frac{1}{r_{ds2}} + \frac{1}{r_{ds1}}} \overset{?}{\approx} -g_{m1}$
  - So effect on is very small

So, "one-sided" cascode does not have a large effect overall

Fully-Cascoded Amplifier





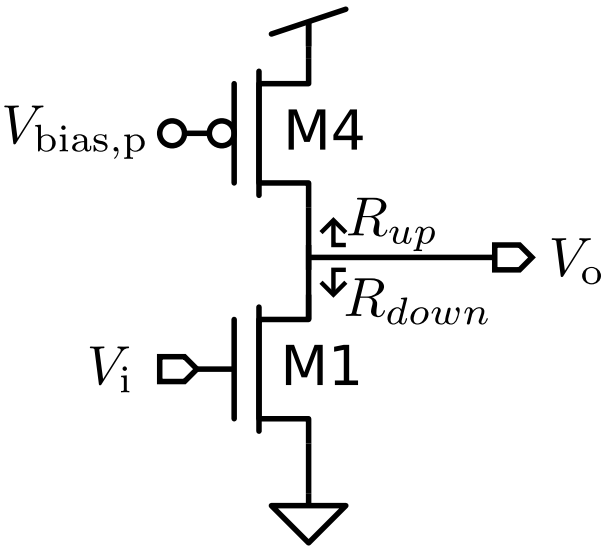
$$R_{out} = (r_{ds3} g_{s3} r_{ds4} + r_{ds3} + r_{ds4}) \,||\, (r_{ds1} g_{s2} r_{ds2} + r_{ds1} + r_{ds2})$$

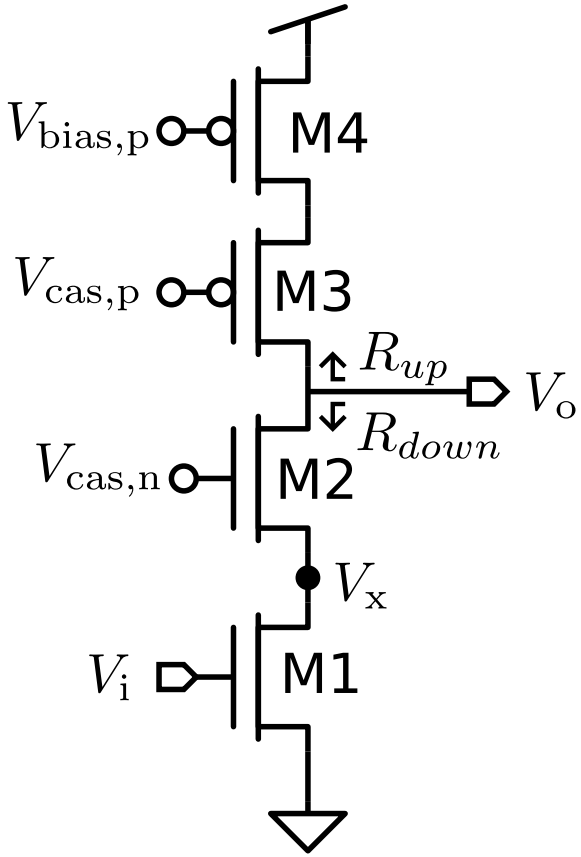
$$R_{out} \overset{?}{\approx} (r_{ds3} g_{s3} r_{ds4}) \,||\, (r_{ds1} g_{s2} r_{ds2})$$

$$R_{out} \overset{?}{\approx} \frac{1}{2} g_s r_{ds}^2$$

$$G_m = -g_{m1} \frac{g_{s2} + \frac{1}{r_{ds2}}}{g_{s2} + \frac{1}{r_{ds2}} + \frac{1}{r_{ds1}}} \overset{?}{\approx} -g_{m1}$$

Fully Cascoded Amplifier





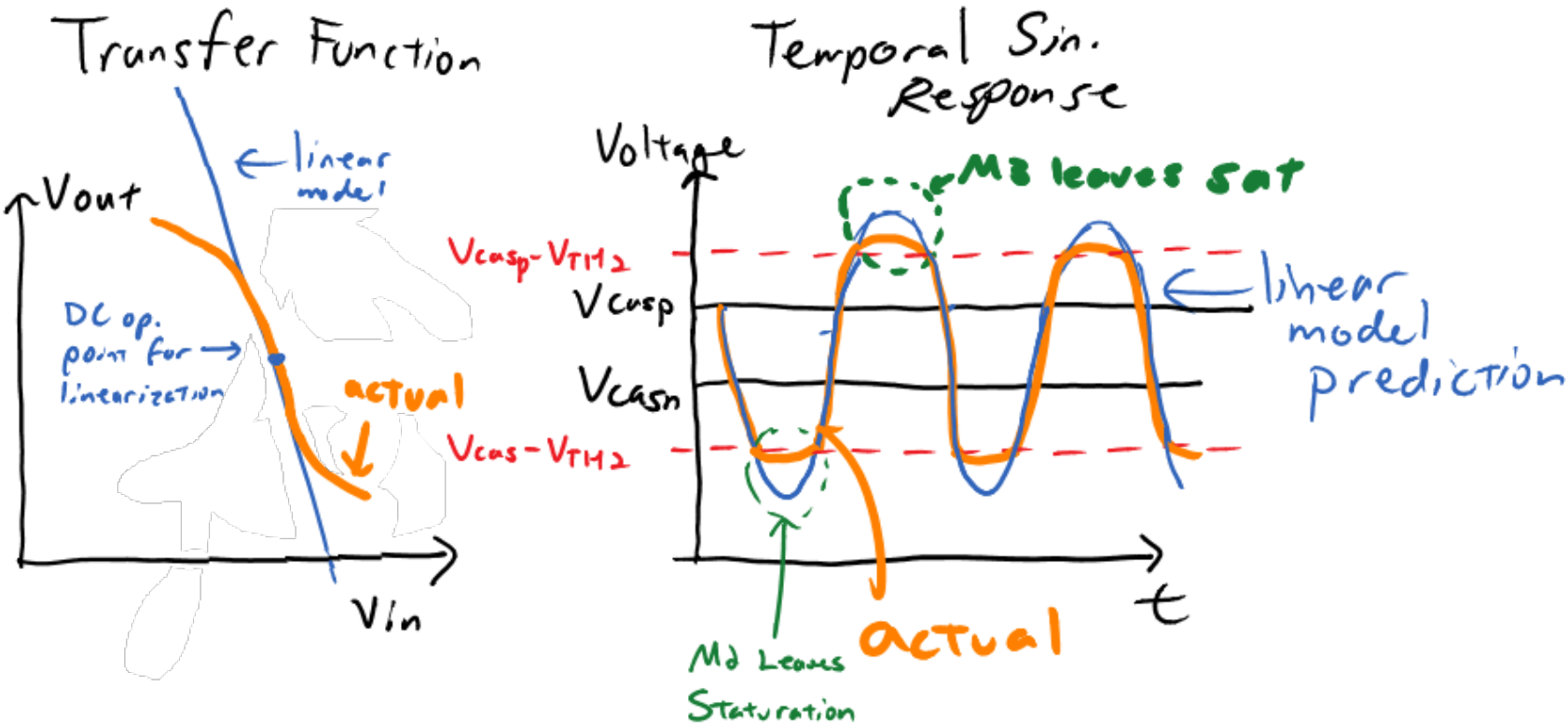
- Non-cascoded: $A_V = g_m \frac{1}{2} r_d$
- Cascoded: $A_{V,cas} = g_m \frac{1}{2} g_s r_{ds}^2$
- $\frac{A_{v,cas}}{A_V} = g_s r_{ds}$
  - (gain multiplied by intrinsic gain)
  - (sometimes thought of as two gain stages)

Output Range

$$V_{casn} - V_{TH2} = V_{out,min} < V_{out} < V_{out,max} = V_{casp} + |V_{TH3}|$$

- Best case allows output to reach within two overdrive voltages of supply rails:
  - If this condition on V_{casn} AND V_{casp} is TRUE:
    - $V_{casn} = V_{TH1} + V_{ov1} + V_{TH2} + V_{ov2}$ and $V_{casp} = V_{DD} - |V_{TH4}| - V_{ov4} - |V_{TH3}| - V_{ov3}$
  - Then:
    - Best case is achieved: $V_{ov1} + V_{ov2} < V_{out} < V_{dd} - V_{ov2} - V_{ov3}$
- I define PFET overdrive voltages as $V_s - V_g - |V_{THp}|$ to keep the values typically positive

DC Transfer Curve



Overall Points for Fully Cascoded Amplifier

- Output range:
  - about a loss of two overdrive voltages (one toward each supply rail) as compared to non-cascoded version
- Gain:
  - multiplied by intrinsic gain
- Rout:
  - multiplied by intrinsic gain
- BW:
  - due to increased Rout, possible loss of BW, divided by intrinsic gain

Circuit Debugging notes/tips:

- M1 not sat:
  - Try increase Vcasn to raise VD1 or
  - decreasing Vov1 or Vov2
- M4 not sat:
  - Try decrease Vcasp to lower VD4 or
  - decrease Vov3 or Vov4
- M2 not sat:
  - try decease Vcasn or
  - decrease Vov2 or
  - decrease Vcasn and Vov1
- M3 not sat:
  - try decease Vcasp or
  - decrease Vov3 or
  - increase Vcasp and decrease Vov4

How to affect a given V_{OV}? Consider $\frac{W}{L}$ and I_{bias}
Note decreasing V_{ov1} means lower input voltage bias point