The functional description of a current mirror is that it should “copy” a current.

\[ I_{\text{out}} = I_{\text{in}} \]

A current mirror can also have a gain \( \alpha \)

\[ I_{\text{out}} = \alpha I_{\text{in}} \]
A good current mirror will have only a small dependence on $V_{out}$:

$$I_{out} = \alpha I_{in} + \beta V_{out}$$

where $\beta$ is ideally ZERO. If $\beta$ is small, $R_{out}$ does not depend on the load.
Basic Current Mirror

Key Characteristics:
- Current Input, Current output
- Rin, Rout
- Input Voltage Range,
- Output Voltage Range
- Gain
- Linearity
Two transistors with the same build and the same gate, drain, source, and bulk potentials conduct the same current.

The gate and drain voltages both have an impact on current, but the gate matters more.
Mirror Node Behavior:

- \( \frac{dV_M}{dt} = \frac{I_{in} - I_{ds1}}{C_M} \)

DC condition:

- \( I_{in} = I_{ds1} = \frac{k'}{2} \left( \frac{W}{L} \right)_1 V_{ov1}^2 \)
- \( V_{ov1} = \sqrt{\frac{2I_{in}}{k' \left( \frac{W}{L} \right)_1}} \)

Feedback Computes Inverse of \( I_{DS}(V_g) \) Function! Answers: “What gate voltage is required to conduct a specified current?”

“Computed” Gate Voltage Applied to M2:

Define: \( V_M = V_{ov1} + V_{TH1} \)

- \( I_{out} = \frac{k'}{2} \left( \frac{W}{L} \right)_2 V_{ov2}^2 \)
- \( I_{out} = \frac{k'}{2} \left( \frac{W}{L} \right)_2 (V_M - V_{TH2})^2 \)
- \( I_{out} = \frac{k'}{2} \left( \frac{W}{L} \right)_2 (V_{ov1} + V_{TH1} - V_{TH2})^2 \)

If \( V_{TH1} = V_{TH2} \),

- \( I_{out} = \left( \frac{W}{L} \right)_1 I_{in} \)
Revisit the assumptions of saturation.

M1:

- \( V_{d1} > V_{g1} - V_{TH1} \)
- (1) Note \( V_{d1} = V_{g1} \)
- (2) \( V_{d1} > V_{d1} - V_{TH1} \) (obviously true if \( V_{TH1} > 0 \))
- \( \therefore V_{d1} > V_{g1} - V_{TH1} \)

**Key Analog Knowledge on Diode-Connected FETs:**

Diode connected transistor in above-Vt operation mode is always in saturation

M2:

- \( V_{d2} > V_{g1} - V_{TH2} \)
- \( V_{out} > V_{ov2} \) \( (V_{ov2} \text{ determined by } I_{out}, W_2, L_2) \)
- \( V_{out} > \sqrt{\frac{2I_{out}}{k'(\frac{W}{L})^2}} = V_{out, min} \)

- Saturation condition constrains allowable output range
Now considering Channel Length Modulation and computing $V_M$ then $I_{out}$ as before:

$$I_{out} = I_{in} \left( \frac{W}{L} \right)_1 \frac{1 + \lambda V_{ds2}}{1 + \lambda V_{ds1}} \left( \frac{W}{L} \right)_2$$

Even if $\lambda_1 = \lambda_2$ and can have $\frac{1 + \lambda V_{ds2}}{1 + \lambda V_{ds1}} \neq 1$ since there is no guarantee that $V_{ds1} = V_{ds2}$. 
Effect of Channel Length Modulation (Effect of Drain Voltage)

Assume: \( W_1 = W_2 = W \); \( L_1 = L_2 = L \); \( \lambda_1 = \lambda_2 = \lambda \)
Examine \( \lambda_1 \) effect with \( V_{DS2} \) held fixed:

\[ R_{in} \] (determines \( \Delta V_M \) in DC):

\[ i_{in} = V_M \left( g_{m1} + \frac{1}{r_{ds1}} \right) \]

- \( R_{in} = \frac{V_M}{i_{in}} = \frac{1}{g_{m1} + g_{sd1}} \)
- \( R_{in} \approx \frac{1}{g_{m1}} \) if \( g_{m1} \gg \frac{1}{r_{ds1}} \)

\( G_{M2} \):
- \( G_{m2} = -g_{m2} \)
Effect of Channel Length Modulation (Effect of Drain Voltage)

\[
\begin{align*}
\frac{dl_{out}}{dl_{in}} &= \frac{dl_{out}}{dV_M} \frac{dV_M}{dl_{in}} \\
&= \left( \frac{1}{G_{M2}} \right) \left( \frac{1}{R_{IN}} \right) \\
\frac{dl_{out}}{dl_{in}} &= \frac{-g_{m2}}{g_{m1} + g_{ds1}} \approx \frac{-g_{m2}}{g_{m1}} \\
&= \text{ideally } \left( \frac{W}{L} \right)_2 \left( \frac{W}{L} \right)_1
\end{align*}
\]

Ideally \( g_{ds1} \) is small so that we can ignore it:

\[
\frac{g_{ds}}{g_m} \propto \frac{1}{\sqrt{\frac{2L}{W}}} = \lambda_0 \frac{L_0}{L} \sqrt{\frac{1}{2}} k' \left( \frac{W}{L} \right)
\]

by keeping \( \frac{W}{L} \) constant and increasing \( L \), the effect of \( g_{ds} \) on the \( V_M \) calculation is reduced

otherwise, the current mirror gain is

\[
K = \frac{g_{m1}}{g_{m1} + g_{sd1}} \quad \text{and} \quad 0 < K < 1
\]

Dr. Ryan Robucci  Lecture VI
Intuitive Explanation for $K$:

- Ideal $\Delta V_M$ is calculated according to inverse of $g_{m1}$.
- When $\Delta V_M$ is calculated according to inverse of $g_{m1} + g_{ds1}$, $\Delta V_M$ is smaller.

So, $g_{ds1}$ causes reduction in output current.

Now examine the current mirror’s behavioral dependence on output voltage.
Examine dependence on output voltage with input current (and \( V_M \)) fixed:

\[
\frac{dl_{out}}{dV_{out}} = (R_{out})^{-1} = (r_{ds1})^{-1}
\]

to make \( l_{out} \) independent of \( R_L \) and \( V_{out} \)

\( R_{out} \) should be large, making \( L_2 \) large helps:

\( R_{out} = r_{ds2} = \frac{1}{\lambda_2 I} ; \lambda_2 = \lambda_0 \frac{L_0}{L_2} \)
Drain Voltage Matching

For best current matching, want $V_{d1} = V_{d2}$ and $L_1 = L_2$ in addition to $V_{g1} = V_{g2}$.

Several non-ideal second-order behaviors are better matched in parallel when transistor dimensions and all voltages match.

as $I_{in}$ increases, $V_m$ increases $\Rightarrow$ $V_{d1}$ increases

$V_{out}$ decreases if set by resistor or is fixed by another load

$I_{out} = I_{in} \left( \frac{W}{L} \right)_1 \frac{1+\lambda V_{ds2}}{1+\lambda V_{ds1}}$ predicts degraded behavior
Drain Voltage Matching

\[ I_{\text{out}} = I_{\text{in}} \left( \frac{W}{L} \right)_{1} \frac{1 + \lambda V_{ds2}}{1 + \lambda V_{ds1}} \]

Since \( V_{DS2} \) and \( V_{DS1} \) can’t match at all currents, may at least achieve \( V_{D1} = V_{D2} \) at some base point given \( V_{out, bias} \) design \( V_{ov1} \):

\[ V_{M} = V_{ov1} + V_{TH1} = V_{out, bias} \]

\[ V_{ov1} = V_{out, bias} - V_{TH1} \]

\[ \sqrt{\frac{2I}{k' \left( \frac{W}{L} \right)^{1}}} = V_{out, bias} - V_{TH1} \]

design \( \frac{W}{L} \)
To increase output resistance, and make the output current less sensitive to output voltage, a cascode can be used:

\[ R_{out} \approx g_s r_{ds}^2 \text{ (good)} \]
\[ R_{in} \approx \frac{1}{g_m} \]

This \( R_{out} \) is good, but let's study the current to current transfer function:
As $I_{in}$ increases,
- $V_M$ increases to support the additional current in M1
- $V_{S4}$ decreases to support the additional current in M4
as a result $V_{d1}$ increases yet $V_{d2}$ decreases

$$I_{out} = I_{in} \left( \frac{W}{L} \right)_1 \frac{1+\lambda V_{ds2}}{1+\lambda V_{ds1}}$$ predicts poor behavior (but not as bad as prev.)

As before, we can at least design M3 to get $V_{D2} = V_{D1}$ at a specified bias current

$V_{D1} \approx V_{ov1} + V_{TH1} = V_M$
$V_{D2} \approx V_{cas} - V_{TH3} - V_{ov3}$
so, set $V_{ov3} = [V_M] + V_{TH3} + V_{ov3} = [V_{ov1} + V_{TH1}] + V_{TH3} + V_{ov3}$
For precision matching biasing:

- \( V_{\text{cas}} = 2V_{ov} + 2V_{TH} \) (big O)
- \( V_{\text{out}, \text{min}} = V_{\text{cas}} - V_{TH3} \)
- \( V_{\text{out}, \text{min}} = 2V_{ov} + V_{TH} \) (big O)

if high \( R_{out} \) is needed rather than precision matching, may set \( V_{\text{cas}} = V_{ov2} + V_{TH3} + V_{OV3} \)

- \( V_{\text{out}, \text{min}} = V_{\text{cas}} - V_{TH3} = V_{ov2} + V_{OV3} \)
- \( V_{\text{out}, \text{min}} = 2V_{ov} \) (big O)
Easy design that generates $V_c$

Since $V_{gs3} \approx V_{gs4}$ and $V_{g3} = V_{g4}$

$V_x \approx V_M$

$\Rightarrow$

The varying $V_c$ keeps lower drain voltages matched

\[ I_{out} = I_{in} \left( \frac{W}{L} \right)_1 \frac{1 + \lambda V_{ds2}}{1 + \lambda V_{ds1}} \]

predicts good current matching behavior

$V_C = 2V_{on} + 2V_{TH}$ (big O)

$V_{out, min} = 2V_{on} + V_{TH}$ (big O)

$R_{in} \approx 2 \frac{1}{g_m}$

Input Voltage: $V_{TH1} + V_{OV1} + V_{TH3} + V_{OV3}$

$2V_{TH} + 2V_{OV}$ (big O)
Wide-Range Biasing

Output Resistance:
\[ R_{\text{out}} \approx g_s r_{ds4} r_{ds2} \]
\[ R_{\text{out}} \approx g_s r_{ds}^2 \text{ (big O)} \]
Input Resistance:
- \[ R_{\text{in}} \approx \frac{1}{g_{m1}} \text{ Why?} \]
  - ✢: Super FET with effective drain conductance \((g_{m3} r_{ds3}) r_{ds1}\)
  - \[ R_{\text{in}} = \frac{1}{g_{m1} + \frac{1}{(g_{m3} r_{ds3}) r_{ds1}}} \]
- Effect of \(V_{g1}\) of on current is much larger than that of a changing \(V_{d3}\) on the cascode structure
Wide-Range Biasing

Lower $R_{in}$ is good for current input port
- less dependence on $V_{in}$
- holds $V_{in}$ fixed
- lowers input node time constant

Output Range:
- $V_{out} > V_{cas} - V_{TH3} = V_{out,min}$
- if $V_{cas} = V_{OV3} + V_{TH2} + V_{OV4} + V_{TH4}$
  - $V_{out,min} = V_{ov2} + V_{TH2} + V_{OV4}$
  - $V_{out,min} = 2V_{ov} + V_{TH}$ (big O)

Input Voltage:
- $V_{in} = V_{ov1} + V_{TH1}$

For both transistors to be in saturation (above-threshold) a lower bound on the input voltage is $V_{in} > V_{ov1} + V_{ov3}$
So, we require $V_{ov3} < V_{TH1}$. Design $(\frac{W}{L})_3$ AND $V_{cas}$ accordingly
Design $(\frac{W}{L})_3$, $V_{cas}$ according to maximum input current
Want $V_{cas} \approx V_M - V_{TH1} + V_{TH3} + V_{OV3}$

$V_{CAS} - V_M = -V_{TH1} + V_{TH3} + V_{OV3} = V_R$

so, set $R = \frac{-V_{TH1} + V_{TH3} + V_{OV3}}{I_{in}}$

then, $R_{in} \approx R + \frac{1}{g_{m1}}$ (derive as practice)

Input voltage: $V_{TH1} + V_{OV1} + V_{TH3} + V_{OV3}$
Other Biasing Circuits (3)

\[ V_{cas} = (V_{TH5} + V_{OV5}) + (V_{TH6} + V_{OV6}) - (V_{TH7} + V_{OV7}) \]

- make \( \left( \frac{W}{L} \right)_7 \) large, so large that \( V_{ov7} \approx 0 \)
- then \( V_{cas} \approx V_{ov} + 2V_{TH} \)
Multiplying Mirrors

Multiplying W’s in output leg creates a current multiplication:

\[ I_{\text{in}} \rightarrow I_{\text{out}} \]

Multiply \( W_2 \) & \( W_4 \) by \( M \)

let \( I_{\text{out}} = M \cdot I_{\text{in}} \)

\[
V_{\text{ov1}} = \sqrt{\frac{2I_{\text{in}}}{k'(\frac{W}{L})_1}}
\]

\[
V_{\text{ov2}} = \sqrt{\frac{2I_{\text{out}}}{k'(\frac{W}{L})_2}} = \sqrt{\frac{2[M \cdot I_{\text{in}}]}{k'[M \cdot (\frac{W}{L})_1]}}
\]

\[ \because \text{biasing is maintained as output leg widths are increased} \]
Bidirectional Current Mirror

\[ I_{\text{out}} = I_1 + I_{\text{in}} - I_2 \]

\[ \frac{\partial I_{\text{out}}}{\partial I_{\text{in}}} = \text{that of the mirror} \]
Active Cascode Current Mirror

Uses feedback to increase output resistance (derived in HW)
Will discuss feedback later.